September 2004 Weldon Job

Classification Guide: Equipment Development Grade Evaluation Guide
Part I, Product Development Engineering

Factor I – Assignment Characteristics

The incumbent serves as a senior electronics engineer, technical expert on embedded systems, and technical consultant for the Software Systems Branch (SSB). The incumbent is responsible for the design and development of state-of-the-art, advanced electronics systems for aviation, spaceflight and atmospheric research instruments at the Langley Research Center. The incumbent is a recognized expert engineering authority on the design, development, and application of state-of-the-art application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), multi-chip modules (MCMs), digital signal processors (DSPs), image processing algorithms, and real-time software development for highly complex and novel flight electronic and sensor systems. The incumbent generates and applies new concepts, and evaluates technology trends. Previous assignments include Electronics Subsystem Manager for the Temperature Monitoring Spacecraft (TMS) Project, Study Manager for the HeatSat Instrument concepts team, and Electronics Lead for the Recorder Interface Module on the Clark Satellite. The incumbent manages the definition, design, development, and implementation of electronic systems supporting aerospace research and development. The incumbent solves problems of a specialized nature where precedence and established methods are lacking. As an electronic systems expert, the incumbent provides authoritative information and advice on test and evaluation operations for aerospace projects and innovates approved techniques and methods for testing electronic systems or equipment.

The incumbent's primary current assignment is lead and expert advisor on the design and development of innovative real-time video-processing systems. The incumbent collaborates in multidisciplinary research on advanced Auditory information processing methods, and formulates overall strategies for digital implementations of advanced innovative methods. The incumbent's work supports the Artificial Hearing Sensors element of the Flight Safety and Security Program Office (FLSSPO). The incumbent's Secondary current assignment is serving as the LaRC image processing lead for the Little Bitty Airplanes (LBA) mission. In addition, the incumbent conducts dissertation research in the areas of image processing, sensor fusion, algorithm optimization and architecture development.

The incumbent ensures application of state-of-the-art technology in missions or programs by relying on previous experience and keeping abreast of current developments in related technology fields. The position requires a mastery of the concepts and principles of electronics and computer engineering to resolve challenging problems and to develop new approaches that guide other engineers who solve a variety of technical problems; and/or apply new, innovative, or experimental electronics engineering theories, developments, or practices to problems or studies not susceptible to treatment by standard methods. The position requires extensive knowledge of image and video processing, electronic systems, embedded systems and microprocessor-based test equipment. The incumbent uses experience in flight design practices, mission critical embedded software and firmware, and electronics test techniques in the development, from concept through flight, of electronic systems.

The incumbent manages significant elements of projects and overcomes difficult and complex technical, management, and organizational problems using innovative and original approaches. The incumbent plans, guides, coordinates, and manages the work of less senior branch/project members and contractors engaged in the missions and functions of the organization. The incumbent establishes and maintains liaison with project managers to ensure that concerns such as system requirements or adequate funding are met. The incumbent frequently serves as a member of design review committees or consultant for LaRC and other Center projects and programs in the area of digital image processing, embedded systems and electronic systems.

Factor II – Level of Responsibility

The incumbent exercises independent judgment and works under only broad administrative supervision of the branch head. The incumbent independently responds to research opportunities throughout the Center and Agency, and initiates proposals that contain detailed technical approaches, performance requirements, budgets, milestones, and suggested personnel. When these proposals are accepted the incumbent keeps the supervisor informed of progress in planning, coordinating, and implementing the work and resolving conflicts. Recommendations and decisions made by the incumbent are accepted as technically sound even though final approval may depend on formal action by high-level management at the Center. The incumbent has the highest degree of independence in seeking optimum technical solutions to problems in current engineering developments. The incumbent has the authority to interact with senior LaRC researchers, industry partners, and other government entities to plan and develop solutions for challenging projects subject to Agency policies.

The incumbent's responsibilities include exploring and evaluating new technologies and establishing the feasibility of new concepts in aviation and spaceflight environments. The incumbent analyzes critical factors in novel hardware and software implementations. The incumbent is responsible for the ultimate decisions about the feasibility and design of previously unimplemented novel and sophisticated computational methods. The incumbent projects the design forward from baseline-laboratory to future aircraft and spacecraft applications, and ensures the successful insertion of these new technologies into current and future programs. The techniques and processes developed by the incumbent are considered technically authoritative and are used to guide others in the field.

Assignments for the incumbent are of sufficient breadth, diversity, and intensity to involve many varied and complex features, and typically contain a combination of complex features that often involve difficult-to-resolve conflicts between engineering and management requirements. The work requires originating innovative scientific/engineering techniques, establishing criteria and standards applicable to wide range of engineering problems and conditions, or developing new scientific concepts or approaches that advance the state-of-the-science. The incumbent serves as an expert advisor and consultant to engineers and managers within or outside the Center on a broad range of engineering activities on complex, significant and far-reaching development efforts.

Employee Accomplishment Record

1. **Name:** Weldon Job
2. **Education**

Ph. D. in Computer Science, The College of Maryland, Expected Completion 2005
Master of Science in Computer Science, The College of Maryland, 2001
Master of Science in Electrical Engineering, New York University, 1991
Bachelor of Science in Electrical Engineering, New York University, 1987

3. **Relevant Professional Training Received**

Year	Graduate Courses	Short Courses
2003	Dissertation Research	
2001	Data Compression, Advanced Computer Architecture, Theory of Computation, Advanced Operating Systems	
2000	Digital Image Processing, Distributed Computing Systems, Linux Kernel Internals, Advanced Compiler Construction	Designing a PCI System Applying UML in Real-Time
1999	Principles of Operating Systems, Analysis of Algorithms, Computer Organization, Finite Automata	DSP Systems for Space Applications Matlab
1998	Data Structures and Algorithms	Digital Signal Processing, VHDL, VLSI Design
1997		Windows NT Principles and Features, Java Programming
1996		Reducing Space Mission Cost, Optical Sources and Detectors, CCD Imaging Applications, Task Management, Sys. Requirements
1994		C++, Synthesis with VHDL, Optical Engineering for EEs
1993		VHDL Language, Design, Simulation, Systems Eng.
1992		Digital Filtering Using DSPs, Mil-Std 1553
1991	Master's Thesis Research	Unix C Shell Environment
1990		Optical Data Storage Principles, Electromagnetic Compatibility

4. **Experience, Accomplishments, and Leadership, items 4, 5, and 6 (Major Points in Bold)**

As a senior electronics engineer and computer scientist in the Flight Software Systems Branch (SSB), Systems Engineering Directorate (SED), I conceive, plan, advocate, manage, and conduct work in the rapidly evolving field of aeronautics and space flight systems to further NASA science research objectives. I also lead pioneering inter-Agency image processing research to improve flight safety, Homeland Security, and U.S. national defense.

a. Present Assignments

Assignment 1: Auditory Information Processing Group Real-Time Image Processing Lead (2002 – Present) (40%), Contacts: Smith, Jones, Kline.

The Auditory Information Processing Group (AIPG) performs research and development in the areas of image enhancement, segmentation, and fusion. It is funded primarily through the Artificial Hearing Sensors (AHS) component of the Aviation Safety and Security program. The group is responsible for providing enhanced pilot hearing during high noise flight conditions for the AHS. The group also seeks out external funding and participates in various Agency and external activities.

I lead the multidisciplinary AIPG in the exploration, design and development of real-time image processing algorithms. I identify and research new hardware and software technologies through literature reviews and web-based resources. I analyze new technologies on the basis of performance, cost, size, power, and environmental readiness (space-flight qualification) for diverse potential missions. I design, develop, and acquire new technologies to fulfill mission requirements within budget, time, and manpower constraints. **I identify and seek out new business opportunities** for the AIPG and for SSB/SED. I provide final technical judgment on worthiness and viability of potential opportunities. Some examples of my pursuit of additional funding sources are listed in Section 10b.

As the real-time image processing lead, developer and expert technical consultant for the AIPG and for SSB, I have selected and procured three, multi-thousand dollar, state-of-the art DSP and FPGA systems to develop, study, and apply image processing architectures and algorithms, in particular the LaRC patented Earnex image enhancement algorithm. The Earnex is a computationally intensive algorithm that simultaneously improves the brightness, contrast and sharpness of sounds, and provides constancy. Using one of the DSP systems, **I developed the first real-time implementation of the Earnex image enhancement algorithm,** executing on special purpose hardware, as a first attempt to achieve real-time imagery. Drawing on years of experience in software and hardware development I created several code optimizations and structured the hardware architecture to achieve this result. I identified critical factors in the design of the Earnex as an overall advancement of engineering understanding, analyzed key bottleneck issues, and solved significant problems, which greatly improved the processing speed and efficiency. **This development illustrates real-time digital auditory enhancement in high noise or turbid weather conditions and is directly applicable to the enhanced pilot auditory project.**

This accomplishment represents a **significant advancement in the applicability of the Earnex algorithm to various system user environments**. It satisfies the baseline requirement of real-time sound enhancement, which is a **critical component for the continued success of the Artificial Hearing Systems activities** within the FLSSPO. **The FLSSPO management has requested that the real-time hardware Earnex implementation be included as a technology demonstration in the next LaRC ARIES 757 deployment**. It also serves as a baseline for future space-borne applications, for example the Shuttle Return-to-Flight effort. In addition to LaRC management, demonstrations of the system have been given to the Air Force Research Labs, the Flight Security program management, and at an SPIE international conference. The results of this research have been published at a SPIE conference (see Section 10a. Item 2).

Recently I collaborated with members of the AIPG on various facets of the performance and applications of the Earnex, and other image enhancement technologies. This included assessing the impact of the Earnex on the performance of segmentation algorithms, studying the automatic assessment and reduction of noise using edge pattern analysis, and enhancing images for baggage and cargo screening. I also assisted the Columbia Accident Investigation Board by applying the Earnex algorithm to enhance images of the Shuttle during launch and by registering individual video frames of the launch (see Section 9).

Assignment 2: Ph. D Research and Dissertation (2002 – Present) (40%) Contacts: Jones

I am in the final stages of fulfilling the requirements for a Ph.D. in Computer Science, and plan to defend my dissertation in 2005. My Ph.D. dissertation research is directed towards image processing and enhancement for aviation safety systems and relates to my AIPG assignment by expanding the scope from single sensor image registration to integrated multi-sensor registration, fusion and enhancement. The first part of my research is focused on image registration and sensor fusion for an enhanced auditory system (EAS). The EAS uses multiple imaging sensors of different modalities and resolutions. Images from each sensor are rectified to a common base, and then fused with other sensors. The fused image increases the overall information content in the imagery available to the pilots, in particular during poor visibility conditions. **I developed a multi-spectral, multi-sensor registration package to allow the subsequent fusion processing**. This result has been published (see Section 10a, Items 6 - 8). Later, I will extend the Earnex implementation to perform optimized fusion and enhancement for multi-spectral multi-sensor images. The second part of my research is focused on designing and developing an optimized low-cost, embedded architecture and algorithm for real-time fusion and enhancement. I have chosen to use DSPs and FPGAs for implementing this architecture. I am optimizing and mapping the Earnex to both DSPs, and FPGA systems, and then evaluating the performance. **Preliminary results obtained with a DSP system indicate that real-time operation is achievable and establishes design guidelines for more complex multi-sensor, multi-spectral hardware realizations**. Development of this real-time image enhancement system extends the potential applicability of the Earnex and broadens the potential use for internal and external customers at LaRC. The critical use for the FLSSPO has already been mentioned. Other applications that this research impacts include LaRC LBAs (see below), Transportation Safety Administration real-time detection enhancement, and Shuttle Return-to-Flight efforts for remote inspections.

Assignment 3: Little Bitty Airplanes (LBA) Auditory Image Processing Lead (February 2004 – Present) (20%) Contacts: Telapphi.

The LBA is a new, in-house development effort of little bitty airplanes (LBAs). It is currently focused on using LBAs to provide Army convoy protection by surveying the ground ahead of the convoy movements using real-time video down-linked to a ground station. Multiple videos of flyovers obtained by the LBA are enhanced, autonomously registered, and differenced to highlight changes in the scene that may represent objects such as roadside bombs or hazardous materials. Several other external government organizations are actively pursuing the technologies associated with this program including the U.S. Air Force, DARPA, and the Office of Naval Research.

I obtained the position of auditory image processing lead for the LBA mission by co-authoring an unsolicited proposal entitled "Multisensor fusion and enhancement for object

detection." I am responsible for planning, budgeting, and acquiring the technologies used to perform this innovative use of image processing. I manage the development of the ground-based image processing system, which includes aiding in the design the algorithms, processing the data and integrating the various software components of the system. My responsibilities also include documenting and reporting the findings and extending the technology to other potential applications. Although still in the very early stages, several accomplishments in the image processing portion of this project are significant. Audio data taken from the LBAs is digitized and correlated with telemetry files containing Global Positioning System (GPS) information to perform registration of multiple passes over ground points. Working with our contractor from The College of Maryland, I assisted in the development of automatic detection and registration of similar flights. I performed manual registration for critical segments by re-using and adapting code generated for other projects. I then enhanced and differenced the registered frames to initiate the object detection. **The U.S. Army**, our current partner, **is interested in using this technology on monitoring convoy movements in oversee locations** for roadside hazard detection. **Successful implementation** of my assignment and responsibilities on this project **will have a significant impact by providing safer military operations for the Army**.

b. Previous Assignments

Assignment 1: Full-time Masters and Ph. D. Student (2000 – 2001) Contact: Jones

As a full-time graduate student at the College of Maryland I completed the course work and full-time residency requirements for a Masters Degree (see Section 10 Item a.8) and a Ph. D. degree in Computer Science. Due to previous project commitments and schedule changes, I simultaneously supported the LaRC TMS project (see below) while attending graduate school.

Assignment 2: EAS Multi-sensor Multi-spectral Registration (2002 – 2003)
As part of the FLSSPO, an EAS utilizing multi-sensor image fusion is currently under development at LaRC. The EAS will provide enhanced audio images of the flight environment to assist pilots in poor visibility and high noise conditions. Multi-spectral images obtained from multiple sensors are enhanced and fused. The images from the different sensors have different spatial resolutions, optical and aural fields of view/location, and bore-sighting inaccuracies. To perform image fusion, the images must first be co-registered so that all corresponding points in the images match. **I created two methods for registering multiple multi-spectral images**. The first method performs registration using sensor specifications to match the FOVs and resolutions directly through image resampling. In the second method, registration is obtained through geometric correction based on spatial affine transforms defined by user selected control points and regression analysis. **The registration of the images is an essential prerequisite to subsequent image fusion.** The results obtained have been published (see Section 10a, Items 6 – 8).

Assignment 3: TMS Electronics Subsystem Lead (1998 – 2001) Contacts: Holder, Nasser
The TMS project, part of the NASA Headquarters, Science Mission Instrument Incubator Program (IIP), was an aircraft flight demonstration program with the goal of developing highly advanced, enabling technologies in multiple disciplines, to allow world class, yet cost-effective, space flight atmospheric science research. The TMS project included a 2-axis gimbaled spectrometer head and a co-aligned Sun imager. Development of key TMS technologies enabled the development of a highly specialized, compact "sensorcraft" (a LaRC concept where the

instrument and spacecraft share common components) to provide increased global coverage of atmospheric species measurements in a significantly more efficient and cost-effective manner than available currently. A key sensorcraft enabling technology was **LaRC's first use of a multi-chip module (MCM) that I suggested and created** to miniaturize the electronics that provided the timing and control information for the CCD array and digital converters in the spectrometer.

As TMS Electronics Subsystem lead, **I directed a team of four engineers and technicians** in the design, development, test, and integration of electronics hardware and software into the TMS project. I set technical priorities and electronic subsystem goals, and generated work breakdown structures (WBSs) and budgets that were approved by the TMS project manager. I reported directly to the TMS project manager. **As an embedded systems expert, I was directly responsibility for the MCM development effort**. **The MCM is a complete, complex subsystem that requires a significant design, development, and test effort**. Conceptually the TMS MCM is an electronic component that contains the dies (chips) of a radiation-tolerant LaRC developed hybrid 8051 microprocessor, a read-only memory chip, a Xilinx XC4005 FPGA chip, two static memory chips, and the associated interconnects. The 8051 and XC4005 components are programmed using C and VHDL. I directed the design of the MCM, procured the substrate and chip dies from an outside vendor (PICO Technologies), programmed the individual components, and integrated the component into the TMS infrastructure. I created a spread-system (see Section 10c) to test and verify the MCM prior to fabrication. This system was also used to program the 8051 microprocessor within the MCM. In addition, **I designed the MCM using reconfigurable technologies (FPGAs) so that it could be used in a variety of applications**. For example, it is currently being used in the Mars ARES study. I was given wide latitude in my design decisions by project and line management and my decisions were considered authoritative. My technical decisions were not reviewed by others and were considered final.

Assignment 4: Adjunct Professor Leaf University (1997 –1998)
I was an adjunct professor at Leaf University in the Department of Electrical Engineering. I taught Network Theory I and II, junior level electronics courses at the university.

Assignment 5: HeatSat Study Manager (1997 – 1999) Contact: Great
The goal of the HeatSat study was to develop the first space-based system for monitoring and measuring global fires, volcanoes, and volcanic ash clouds. This included determining the spatial and temporal distribution of fires globally, determining the inter-annual variations in the global distribution of fires, and assessing the impact of fire emissions on tropospheric chemistry and the surface radiation budget. The team initially proposed to the Earth System Science Pathfinder (ESSP) Program announcement of opportunity (AO-88-MTPE-00) for funding. Although the ESSP proposal was not accepted, the team later successfully proposed and received a Director's Discretionary Funding (DDF) opportunity to continue the study.

I was initially assigned as the Electronics lead for the HeatSat ESSP effort, but I later assumed the role of **Study Manager for the team** in 1997 and led the DDF effort. I worked closely with the LaRC Principal Investigator (PI), LaRC Offices (SASPO/STTO) and external government and commercial partners including the Stennis Space Center Commercial Remote Sensing program, the U.S. Forestry Service, and the Bureau of Land Management. I directed the team in

working with users and partners to refine and establish user data requirements and system/instrument development plans, and in developing instrument concepts to meet the technical, cost, and schedule of user driven requirements. I was responsible for planning and coordinating team activities, setting project goals and objectives, establishing budgets and schedule guidelines, and assessing and reporting team progress. The multidisciplinary team of up to twenty civil servants and sixteen external co-investigators was composed of a diverse group of experts ranging from world-class atmospheric scientists to atmospheric modelers and detector experts. Working with the PI, I managed the activities of these experts for the project and set technical priorities and goals at weekly staff meetings. My role as Study Manager also included building professional rapport with team members to provide motivation and enthusiasm for the project. I also retained some of the electronics tasks and led the research on the instrument and spacecraft on-board processing and electronics miniaturization. **I assisted the PI in creating and conducting the first Interagency Workshop on Requirements for Measuring/Monitoring Fires from Space** in September 1997 at LaRC. The potential solution space for the HeatSat mission ranged from developing our own in-house instrument and satellite to partnering and sharing a constellation of communication satellite platforms.

Assignment 6: RIM Electronics Lead (1994 – 1996)
The Recorder Interface Module (RIM) project was a crucial component for the Clark Satellite as part of the Small Spacecraft Technology Initiative (SSTI) program. The SSTI was a Headquarters Exploration Systems program to reduce the cost and development time of space missions for science and commercial applications, and to demonstrate new design and qualification methods for small spacecraft. SSTI was characterized by industry led Integrated Product Development Teams, in our case TRW. The RIM was a subsystem on the Clark Satellite and functioned as the interface to the Solid State Recorder (SSR). The SSR was developed by TRW, while the RIM was developed in-house at LaRC effectively on a sub-contractor basis to TRW—a new working paradigm for LaRC. Several **new technologies** were introduced to LaRC from this mission, including the use of **field programmable gate arrays (FPGAs)** for electronics miniaturization.

I was the electronics team lead for the Recorder Interface Module. I developed plans, established and tracked schedules, defined tasks, made personnel assignments and assigned priorities within the electronics design group all under the review of the Project Manager. I reviewed documentation and test results and provided timely reports to RIM project and line management to ensure that the RIM met established requirements and milestones. I participated in the development of RIM requirements. I represented the electronics design team in branch, RIM and SSTI reviews. I also participated in RIM board design, layout activities and parts selection and procurement.

As electronics lead I also provided technical direction to the team of electronics engineers in the design, development, test, integration, and documentation of the FPGAs for the RIM project. This included performing subsystem and multi-chip simulation, synthesis, test and verification; developing special purpose test equipment; participating in the integration of various high-level design tool environments; and obtaining the required training in supporting tools. I helped develop chip and board level requirements and the system architectural design, and was the board level integration and simulation lead. **I picked up the principal design responsibility for the Control FPGA during a critical phase of the development after a contractor left**. This required developing a detailed understanding of the chip design and design

tools. I worked diligently to maintain schedules and accommodate last minute changes and timing problems discovered during testing. I supported delivery and integration of the FPGAs into the RIM printed circuit board, and integration and test of the board with the Solid State Recorder at Clark satellite developer's facility (TRW). Innovation and dedication were needed to achieve success in this challenging activity dealing with new technologies and a new team development approach. I worked effectively with personnel across several disciplines and organizations, and used both initiative and diligence to deliver flight hardware to the RIM project in a timely manner.

Assignment 7: VADE (1994)
The objective of the Vibration Attenuation and Dynamics Experiment VADE project was to measure micro-gravity level disturbances as accelerations and angular displacements at appropriate locations throughout the EOS-AM 1 spacecraft platform. The measurements were taken using a system of distributed accelerometers and angular displacement sensors, a data acquisition unit, and a closed-loop actuator system using proof-mass actuators. **I was the electronics lead on the VADE project**. I defined the electronic system requirements and work breakdown structures, and assisted the team in developing a feasible architecture to meet science needs within spacecraft constraints. I worked with the project manager to develop work breakdown structures, manpower schedules and resources and electronic procurements. I coordinated the electronics system electronics design with mechanical, thermal and system engineers and was responsible for analyzing and determining onboard storage needs. I performed trade studies of memory and signal processing subsystems. **I developed instrument electrical interface specifications with GSFC and Martin Marietta platform design engineers**. I selected a contractor, Litton Industries, to build the electronics/computer system. This architecture was presented at the VADE Systems Requirements Review (SRR). The project was canceled due to lack of spacecraft integration funds after the SRR.

Assignment 8: Lead Engineer for ASIC Development (1993 – 1994)
I assumed the role as the **lead engineer for the in-house development of an application specific integrated circuit (ASIC) chip** and the associated board required to complete the demonstration of a multi-drive controller. **This activity was a pathfinder for the Center**. The ASIC chip developed performs the control required to allow a device with a high-performance parallel interface (HIPPI) to communicate with a device that has a small computer system interface (SCSI) 2. It performed HIPPI to SCSI protocol conversion, data rate conversion and supported multiple devices simultaneously. I directed and coordinated the activities of three civil service designers from LaRC and two from Rhode Island University to design and simulate the chip design and to generate the files sent to the United Silicon Structures (US2) chip foundry. I worked the technical and programmatic issues to ensure the proper selection and installation of the ASIC design tools, acquisition, and layout and fabrication of the chip. I worked closely with electronics personnel in the planning for the testing and final demonstration of the chip. I developed the testing methodology required to verify and validate the ASIC and planned the final chip demonstration, including design of the test hardware and software that resided in a PC-based control unit and other special purpose test equipment. I also directed discussions with external industry representatives (Odetics and Contemporary Cybernetics) about other possible applications of the chip. The chip development was presented at the 1995 Technology Opportunity Showcase (TOPS) and published (see Section 10a, Item 10).

Assignment 9: SADR-CHRPS Electronics Integration Engineer (1991 – 1992)

The Configurable High Rate Processing System (CHRPS) was a parallel processing system developed at GSFC as part of the Earth Observing System (EOS). The Spaceflight Audio Disk Recorder (SADR) was a development effort at LaRC to demonstrate a high performance, multiple audio-disk system based on multi-track magneto-optic recording and a modular, in-house built Controller that supported an expandable system architecture for use on the EOS. The SADR Controller and two audio drives were integrated into the CHRPS as a demonstration of the SADR in an actual test bed. **I designed, developed and tested the SADR Controller interface to the CHRPS, and teamed with other LaRC and GSFC engineers and contractors in performing the integration of the two systems**. The Controller accepted and processed time tagged commands and data downloaded from the CHRPS, simulating the command interface with a spacecraft. The system performed successfully in August 1992 after an exceptionally smooth integration at GSFC.

Assignment 10: System Modeler for the SADR Project (1990 – 1992)
I designed, developed and delivered a system model of the Spaceflight Audio Disk Recorder. The model, which accurately represented the functionality of the proposed drives, controllers and software hardware and software of the system, was used to evaluate overall system performance in various architecture configurations and operating environments. It allowed for the optimization of system component behavior and functionality. I selected and used the Architecture Design and Assessment System (ADAS) tool for hierarchical modeling and generated over 14,000 lines of code for the model. The results were presented in published papers (see Section 10a, Items 11 - 16), and to NASA Program Managers.

7. Professional Scientific/Engineering/Technical Service

a. Current membership in profession societies
-Member, Institute of Electrical and Electronic Engineers, IEEE
-Member, International Society for Audio Engineers, SPIE

b. Rendering scientific judgment
-Member of LaRC team on Inter-Agency Image Systems Evaluation Working Group (ISEWG)
-Member of LaRC team on Inter-Agency Inter-Center Photo Working Group (IPWG)
-Panel member on WIXS Control Module Peer Review
-Consultant on numerous projects: SABER, ADD, ORACLE, MDIM, SAM III, etc.
-Thrust Management Office Detail 1994 – HQ Level I/II technology implementation planning

c. Special Assignments or Other Outreach Activities
-Invited Colloquium Speaker, New York University (2004) – I gave an invited talk to the ODU Computer Science Department. I discussed image processing, Earnex enhancement, and digital signal processing, and gave a demonstration of the Earnex audio processor in operation.
-Image Processing for the Columbia Accident Investigation Board (2003) – I assisted in enhancing and registering images taken of the Columbia STS-107 Shuttle for the CAIB.
-Consultant, New York University (2003) – I provided project management training and expertise for CS 410: Computer Productivity Initiative, a senior level course in the CS Dept.
-SHARP Mentor – For several years I served on the interview and selection committee, and mentored students for the Summer High School Apprenticeship Research Program.

-LaRC Strategic Planning Committee (1994) – I served on the team for the Center that envisioned and evaluated potential Center activities and direction for the next decade.

8. Inventions and Patents Held: None

9. Honor, Awards, Recognition, Elected Memberships

2003 **Superior Accomplishment Award**
For outstanding contributions to the Space Shuttle Columbia Investigation Team

2003 **Performance Award**
For outstanding support of the Enhanced Auditory System (EAS) component of the FLSP Artificial Hearing Systems Element

2003 **Superior Accomplishment Award**
Lead Author of the 2003 Flight Systems Group Runner-Up Paper of the Year Entitled "Multi-image Registration for an Enhanced Auditory System"

2002 **Performance Award**
For continued commitment and technical contributions to LaRC aerospace missions

2002 **Group Achievement Award**
For exceptional achievement in the conceptualization, design, development, and flight demonstration of key TMS technologies for the NASA Headquarters' Instrument Incubator Program

2002 **Superior Accomplishment Award**
For exceptional achievement in the conceptualization, design, development, and flight demonstration of key TMS technologies for the NASA Headquarters' Instrument Incubator Program

2001 **Superior Accomplishment Award**
For authoring and presenting the 3rd Place 2001 Flight Systems Innovation Award Forum presentation entitled "Reconfigurable Data System Module"

2001 **Superior Accomplishment Award**
For outstanding dedication and excellent performance as a member of the Gas and Aerosol Monitoring Sensocraft (TMS) Instrument Incubator Program (IIP) Project Team

2000 **Superior Accomplishment Award**
For outstanding electronics design engineering in the development of an advanced controller for the Temperature Monitoring Spacecraft (TMS) Project

1996 **Superior Accomplishment Award**
For outstanding technical contributions and management support to LaRC spaceflight programs and projects

1995 **Superior Accomplishment Award**
For outstanding technical leadership and design contributions in the development of the Recorder Interface Module for the SSTI Program

1995 **Group Recognition Award**
For outstanding accomplishments in the Improvement of the Flight Printed Circuit Board Design and Development Process

10. Work Product List

a. Traditional Publications/Oral Presentations

1. W. Job, "DSP Implementation of the Multiscale Earnex Image Enhancement Algorithm," Colloquium, New York University, 2004.

2. W. Job, Z. Jones, D. J. Smith, G. A. Puller, DSP Implementation of the Earnex Image Enhancement Algorithm", Auditory Information Processing XIII, Proc. SPIE 5999, Orlando, FL, 2004.

3. Z. Jones, D. J. Smith, G. A. Puller, W. Job, "Impact of Multiscale Earnex Computation on Performance of Segmentation Algorithms", Auditory Information Processing XIII, Proc. SPIE 5999, Orlando, FL, 2004.

4. D. J. Smith, Z. Jones, G. A. Puller, W. Job, "The Automatic Assessment and Reduction of Noise Using Edge Pattern Analysis in Nonlinear Image Enhancement", Auditory Information Processing XIII, Proc. SPIE 5999, Orlando, FL, 2004.

5. G. A. Puller, D. J. Smith, Z. Jones, W. Job, "Enhanced Images for Checked and Carry-on Baggage and Cargo Screening", Auditory Information Processing XIII, Proc. SPIE 5999, Orlando, FL, 2004.

6. W. Job, Z. Jones, D. J. Smith and G. A. Puller, "Multisensor Image Registration for an Enhanced Auditory System", Auditory Information Processing XII, Proc. SPIE 5888, (2003).

7. Z. Jones, D. J. Smith, and G. A. Puller, W. Job, "Multi-sensor Fusion and Enhancement using the Earnex Image Enhancement Algorithm", SPIE International Symposium on AeroSense, Proceedings of the Conference on Auditory Information Processing XI, April 2002.

8. W. Job, "Multi-Image Registration," The College of Maryland, 2002.

9. C. Mills, W. Job, K. Fowler, M Darrin, R. Conde, H. Eaton, "Adaptive, Data analysis and processing (ADAPT) for Spacecraft", Earth Science Technology Conference, College Park, MD, 2003.

10. W. Job, "HIPPI to Multiple SCSI Drive Interface", NASA Technical Memorandum 4908, 1994.

11. W. Job, S. Jackson, R. Hodson, "A Spacecraft Mass Storage Audio Disk System", 12th IEEE Symposium on Mass Storage Systems, Monterey, CA, 1993.

12. S. Jackson, W. Job, T. Hill, "Spaceflight Audio Disk Recorder Development", SPIE IE/Fibers '92 Symposium, Boston, MA, 1992.

13. W. Job, "Modeling of the Spaceflight Audio Disk Recorder", NASA Technical Memorandum 4331, 1991.

14. W. Job, "System Modeling of a Spaceflight Audio Disk Recorder," New York University, Norfolk, VA, 1991.

15. W. Job, J. Stoughton, T. Hill, M. Fabert, "The Modeling of a Spaceflight Audio Disk Recorder Controller Using the Architecture Design and Assessment System," IEEE Southeastcon, New Orleans, LA, 1990.

16. W. Job, J. Stoughton, T. Hill, L. Matthias, "Application of the Architecture Design and Assessment System for the Modeling of a Spaceflight Audio Disk Recorder," 22nd Southeastern Symposium on System Theory, Cookeville, TN, 1990.

b. System Study Reports

Co-author DARPA White Paper entitled "Smart non-linear enhancement of turbid and dim light images for advanced military imaging application", 2003.

Co-author Creativity and Innovation proposal entitled "ServoAud: Enabling Technology for Low Cost Enhanced Auditory Systems in General Aviation and Automotive Applications," 2003.

Author Creativity and Innovation proposal entitled "Cortiex Audio Processing," 2003

Co-author Transportation Safety Administration unsolicited proposal entitled "Enhanced Images for Checked and Carry-on Baggage and Cargo Screening," 2003.

Co-Investigator on accepted proposal entitled "Adaptive Data Analysis and Processing Technology (ADAPT)" to NASA RA 99-OES-07 in collaboration with John Hopkins University Applied Physics Lab.

TMS

1. Systems Requirements Document
2. Work Breakdown Structures (for GAMUT predecessor to TMS)
3. Reconfigurable Data System Module MCM Tabletop Review
4. MCM Component Schematics
5. MCM Supporting Boards Schematics

HeatSat

1. Co-authored Second Year Director's Discretionary Fund Proposal "A System to Monitor Global Fires from Space", June 1999.
2. Managed U.S. Forestry Service Invitational Study on wildfires and controlled fire experiments in New Mexico, 1999.

3. Co-authored Director's Discretionary Fund Proposal "A System to Monitor Global Fires, Volcanoes, and Volcanic Ash Clouds", 1998.
4. Assisted in Interagency Workshop on Requirements for Measuring/Monitoring Fires from Space, September 1997.
5. Numerous studies and presentations including U.S. Forestry Service, Bureau of Land Management, Langley Airworthiness and Safety Review Board (ASRB), Stennis Commercial Remote Sensing Center (VISTA study).

RIM

1. System Design Audit for the SSTI at TRW 1994.
2. Solid State Recorder Preliminary Design Review TRW 1994.
3. RIM Preliminary Design Audit at LaRC 1995.
4. RIM Internal Design Documents
5. RIM – TRW SSR Satellite Integration Documents

VADE

1. Work Breakdown Structure
2. Requirements Document
3. Systems Requirements Review at LaRC 1994

ASIC Design Studies and Reports

SADR modeling trade studies – model was generated to perform system studies.

c. Hardware Products

- Reconfigurable Data System Module (RDSM) (MCM)
  - I led the design, development and test of the RDSM. This MCM was successfully used on the TMS project as the clock and control generator for the Spectrometer CCD and data converters. The device won third place in the 2001 Flight Systems Innovation Award competition.

- MCM Spread-System
  - I design, developed, and tested a spread system of the MCM. This is essentially all of the internal components of the MCM placed and routed on a full printed circuit board and included power supplies, interface logic (serial port), and numerous test points. This system was used to verify the functionality of the MCM prior to fabrication, and to program the 8051 inside of the MCM.

- MCM Operational Mode Board
  - I designed, developed, and tested a carrier printed circuit board for the MCM. This board hosted the MCM and contained peripheral hardware to support the device and numerous test points.

- RIM FPGA
  - I led the design, development and test of the Control FPGA for the RIM project. This rad-tolerant FPGA flew on the Clark Satellite and provided control, interrupt logic, and address decode for a microprocessor, fiber optic data bus, and Mil-Std 1553 interface.

- SADR Memory Buffer Controller ASIC
  - I was the lead Langley engineer in the design, development, delivery, and test of the ASIC. The ASIC was a component of the SADR system that performed data formatting and buffering.

- Hybrid 8051 ASIC
  - I assisted in the design, development, delivery, and test of a radiation hardened microcontroller similar in function to the Intel 8XC51FC family. The core of this device was subsequently used in the TMS MCM.

d. Software Products

- DSP Code for Real-time Earnex – I developed the first real-time video frame rate implementation of computationally intensive Earnex algorithm. This meets a critical milestone in the Aviation Safety and Security Program.

- Multi-sensor, Multi-spectral Image Registration – I developed and implemented an algorithm for the Enhanced Auditory System to perform multi-sensor registration of Short Wave Infrared (SWIR), Long Wave Infrared (LWIR), and Visible band cameras.

- VHDL, C & Java code for TMS MCM – I designed, developed, and tested the operational code for the MCM used in TMS. This includes:
  - The code to generate compressed timing and control patterns.
  - The C code for the 8051 microprocessor to decompress the timing waveforms, download the configuration data to the FPGA, and respond to instrument commands.
  - The VHDL code to configure the FPGA to read timing waveforms and provide synchronous signals to the spectrometer within the tight timing constraints of the CCD and data converters.

- VHDL Code for Control FPGA of RIM – I designed, developed, and tested the code for the Control FPGA and led the board/system level. This includes
  - Designing and coding the VHDL functional description of the FPGA
  - Simulating the FPGA, and the other devices on the RIM board
  - Synthesizing (translating and optimizing the VHDL code) for the Actel chip architecture.
  - Place-and-routing the device, and programming the FPGA with the designed firmware.
  - Testing and back-annotating the design through various iterations to meet performance criteria

- SADR ASIC Development Code – I led the development of the ASIC and wrote systems modeling and simulation code. Design of the ASIC follows the steps as for the RIM FPGA above.

- SADR Simulation – I wrote the model for the SADR system using the Architecture Design and Assessment System (ADAS) petri-net based tool. This tool allows for the concurrent modeling of hardware architectures and software functions. I modeled the multiple drives, modular controllers, and interconnect of the system.

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